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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Gregory C. DeSalvo et al. Group Art Unit: 2823
Serial No.: 10/034,723 Examiner: JULIO J. MALDONADO
Filed: 03 January 2002
For: STIFFENED BACKSIDE FABRICATION FOR MICROWAVE RADIO FREQUENCY WAFERS

DECLARATION UNDER 37 CFR 1.132

Honorable Commissioner of Patents and Trademarks

Washington, D. C. 20231

Sir:

I, Gregory C. DeSalvo, declare:

1. That I am employed by the Northrop Grumman Corporation in the city of Baltimore, Maryland USA and was formerly an employee of the United States Air Force in the capacity of a semiconductor device Electronics Engineer at the Sensors Directorate of the Air Force Research Laboratory located at Wright–Patterson Air Force Base, Ohio, 45433-7322.

2. That my educational background includes a Bachelor of Science Degree in Electrical Engineering from Rice University in 1982, a Master's degree in Electrical Engineering from the University of Delaware in 1985, and a Doctor of Philosophy Degree in Electrical Engineering from the University of Delaware in 1989.

3. That I have been working in the field of periodic table group III–V compound semiconductor material growth and device fabrication process development since 1982, and have published several journal articles relating to differing aspects of this work. My specialization in this work has been in the areas of semiconductor photolithographic processing techniques and semiconductor material etching.

4. That I understand five United States patents have been identified as prior art reference patents possibly precluding the issuance of our captioned STIFFENED BACKSIDE FABRICATION FOR MICROWAVE RADIO FREQUENCY WAFERS application as a Letters Patent of the United States in view of the obviousness provisions of 35 U.S.C. 103(a). These references include a primary reference US Patent 6,162,702 of Morcom et al. and the secondary reference US Patents 5,528,080; 6,297,131; 6,358,762 and 5,463,246 of Goldstein, Yamada et al., Kohno et al. and Matsunami respectively. I generally understand the technical contents of the five patents involved in this rejection and desire to herein offer statements of explanation and distinction regarding certain aspects of the invention described in our captioned application and these patents.

5. With respect to the primary reference patent of Morcom et al. I understand this patent to concern semiconductor devices of the "vertical power device" type as are fabricated primarily from Silicon semiconductor material and are provided with backside ribbing of several possible configurations. It appears significant to me that this patent includes no recitation concerning the processing of microwave or other radio frequency signals and in fact is directed to what I understand to be the much lower in frequency "vertical power devices". In keeping with this absence of radio frequency signals, the Morcom et al. patent also includes no between-surface-layer conductors or via elements as we find necessary in order to obtain sufficiently low

ground plane impedances and achieve usable semiconductor device characteristics at microwave frequencies. Our substrate thinning invention is in fact prompted by a need to amplify and communicate such microwave radio frequency signals and therefore includes via elements (with the few milliohms of electrical resistance they provide), surface mounted rather than vertically mounted semiconductor devices and other structure needed to provide desirable microwave amplifying characteristics.

The significance of via elements in radio frequency integrated circuit usage can be further appreciated from the fact that it has become current practice to locate such via elements, and their interconnection of two different wafer surface-located conductors, directly under the source element of a grounded-source field effect transistor (i.e., a transistor is fabricated directly over a via element) in order to achieve the lowest possible impedance in the transistor source electrode current path.

The rejected claims of our application include both preamble and claim body recitations of radio frequency signals and via elements. In view of the absence of via elements and microwave frequency signals in the Morcom et al. patent it therefore appears reasonable to me that this patent be most fairly considered as both non analogous art and a teaching away from the overall combination included in our invention.

7. The use of conventional silicon etching to remove semiconductor material intermediate the grid pattern of the Morcom et al. wafer is another area of significant difference with respect to our invention. Although such conventional etching may be satisfactory in the case of the Morcom et al. silicon semiconductor, we find such etching to be grossly impractical in the case of our materials and the thickness reduction we need to achieve. At best we estimate such conventional etching would require many tens of hours, probably 70 to 100 hours, to accomplish for each wafer processed. We therefore have avoided such conventional etching in favor of the faster inductively coupled plasma (ICP) process we have disclosed. Even though the Kohno et al. reference relied upon in the Office Action discusses the ICP process this does not alter the fact that the Morcom et al. patent teaches away from the ICP combination recited in our claims and is thus subject to an additional question as to its appropriateness as a reference against our application.

8. With respect to the secondary reference patent of Goldstein et al. I understand this patent to concern the fabrication of wafer conductive paths by way of thermally migrated alloy passed partly through a body of semiconductor material. More specifically Aluminum is migrated through Silicon semiconductor in the Goldstein et al. conductive paths. Several aspects of this process appear significant to me; especially since the resulting conductive interconnection elements (94 in the Goldstein et al. patent) are composed of an alloy of silicon and metal materials and only partially pass through the semiconductor layer. There are no via elements, in the true sense of a via element, disclosed in the Goldstein et al. patent. The Goldstein et al. conductors cannot provide the low resistance electrical conduction we need in our invention in view of their higher resistivity and their less than complete pass-through of the semiconductor material. It is interesting that the Goldstein et al. patent does not disclose the achieved interconnection resistance values nor the resistivity achieved in the bulk material of the alloy interconnection elements. The rejected claims of our application include recitation of via holes, via hole intrusions extending through the semiconductor, metallization in via holes, metal to metal connections at via holes,

9. Additionally the Goldstein et al. patent is another example of processing signals other than microwave or radio frequency signals. In this instance there is identification, in at least two locations, of data processing circuitry as the probable application of the apparatus described in the Goldstein et al. patent. Absence of signals of the frequency range processed in our invention in the Goldstein et al. patent appears significant to me and suggests this patent is most fairly considered as non-analogous art with respect to the invention of our application and also as a teaching away from the concepts of our invention.

10. In addition, the temperatures recited in the Goldstein et al. patent for accomplishing annealing and metal alloying and migration into the semiconductor wafer are grossly excessive for the periodic table groups III-V materials we need for our microwave radio frequency devices. These temperatures above 1000 degrees Celsius (e.g. "1200 degrees Celsius for 12 hours" at column 5, line 11) are perhaps compatible with the silicon semiconductor materials disclosed in the Goldstein et al. patent but would be destructive to our needed groups III-V materials. It is also interesting that the Goldstein et al. patent does not include even a "laundry list" recitation of other semiconductor materials usable with their invention. It appears reasonable to me that

attempts to modify the Goldstein et al. invention for use with other semiconductor materials, including our groups III-V materials, would involve at least experimentation that is beyond being routine and performable by a person of ordinary skill in the semiconductor device art. I believe the Goldstein et al. patent is thus fairly considered to destroy the function of our invention, teach away from the concepts of our invention and comprise non-analogous art with respect to our invention.

9. I also believe the Goldstein et al. process of migrating metal directly into an integral semiconductor wafer without first providing a via path or other opening into the semiconductor wafer is not applicable to our invention. My experience suggests it is impractical or impossible to have such alloyed semiconductor and metal "interconnection" diffusions 94 proceed through the standard 100 micrometers thick insulating regions associated with the Monolithic Microwave Integrated Circuits of our invention. Moreover as stated at column 3, line 28 in its text, the Goldstein et al. patent advocates "only the partial migration of the conductive material into the semiconductor body, but not the complete migration through the semiconductor material". Notably the Goldstein et al. patent also does not disclose either a wafer thickness or a length dimension for the migrated interconnecting conductors 94. These differences appear to support at least the non-analogous art and teaching-away conclusions with respect to the Goldstein et al. patent.

10. Additionally, the Goldstein et al. patent specification, in the lower lines of column 1 and the upper lines of column 2, discusses the fabrication and use of conventional via elements in a semiconductor substrate. Since this discussion is followed by disclosure of the Goldstein et al. thermomigration feed through conductors and a lengthy discussion of the purported advantages of such conductors in several possible forms, it appears the Goldstein et al. patent is fairly construed as providing a teaching against use of via hole elements and thus a teaching against the structure we have found to be desirable in our microwave radio frequency devices. Again we have clearly recited such via elements in our rejected claims.

11. The Goldstein et al. patent also appears to teach away from the use of a common material as the through-wafer conductor and as the surface conductor of the semiconductor wafer. We have found this common metallization to be both economical and providing of desirable integral joint-free electrical properties in our invention, however, in the Goldstein et al. patent the surface conductors are made of a metallic material such as the preferred aluminum and the through-wafer conductors are made of a metal and semiconductor alloy. This difference again appears reasonably construed as a teaching away from our invention or a non-analogous art indication in the Goldstein et al. patent.

12. By way of summarizing and emphasizing certain of the above concepts, for any high frequency analog or non-digital integrated circuit such as a Monolithic Microwave Integrated Circuit, operable in the 1 Gigahertz or higher range, it is essential to provide: (a) a thinned insulating region directly under the circuit elements with (b) an accompanying backside ground plane of good electrical conductivity--in order to minimize radiative losses occurring at the high frequencies, and (c) minimal electrical inductance between frontside circuitry and this backside ground plane, achieved by using via holes. All three of these components a, b, and c are needed in combination to reduce losses associated with high frequency circuits. One of these components alone, such as a thinned substrate, without the other components does not achieve a useful, practical, low loss, high frequency integrated circuit. I do not believe any of the identified reference patents disclose the achievement of these three components nor that they include a suggestion of their combination in order to achieve the three components and a useful, practical, low loss, high frequency integrated circuit.

13. It is difficult for me to appreciate how the Goldstein et al. patent adds useful value to or is relevant to the Monolithic Microwave Integrated Circuits and Radio Frequency Integrated Circuits in our invention. No-one processes wafers using temperatures of 1100° C where the wafer includes frontside metal deposits from a previous step because Gold, melts at ~1064° C, Aluminum, melts at ~660° C, Copper, melts at ~1084° C, and Silver, melts at ~961° C. Therefore each of these metals when used in a Silicon or other wafer frontside circuit will re-melt, flow and diffuse and thus destroy the frontside circuit, if the circuit is exposed to temperatures in the 1100° C range. To use the Goldstein et al. process one would have to completely change the normal frontside processing - whether a digital or analog circuit. This method is totally impractical from a processing viewpoint.

14. For standard via hole processing, gold metal is used to provide a low electrical resistance connection between the backside and the frontside of a wafer. Our resistance measurements show achievement of a typical "via hole" resistance between 0.5 and 2 milli Ohms or 0.0005 and 0.002 Ohms for this purpose. The Goldstein 5,528,080 patent, in addition to the previously stated problems with 1100°C high processing temperatures, can in no way provide such low electrical resistance. Therefore I believe this difference also suggests the Goldstein et al. patent is fairly considered as non-analogous art, art that also would destroy the function of our invention and a teaching away from the concepts of our invention.

15. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Gregory C. DeSalvo

29 Dec 03

Gregory C. DeSalvo
Baltimore, Maryland

Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Honorable Commissioner of Patents and Trademarks

Washington, D. C. 20231

Sir:

I, Gregory C. DeSalvo, declare:

1. That I am employed by the Northrop Grumman Corporation in the city of Baltimore, Maryland USA and was formerly an employee of the United States Air Force in the capacity of a semiconductor device Electronics Engineer at the Sensors Directorate of the Air Force Research Laboratory located at Wright–Patterson Air Force Base, Ohio, 45433-7322.

2. That my educational background includes a Bachelor of Science Degree in Electrical Engineering from Rice University in 1982, a Master's degree in Electrical Engineering from the University of Delaware in 1985, and a Doctor of Philosophy Degree in Electrical Engineering from the University of Delaware in 1989.

3. That I have been working in the field of periodic table group III–V compound semiconductor material growth and device fabrication process development since 1982, and have published several journal articles relating to differing aspects of this work. My specialization in this work has been in the areas of semiconductor photolithographic processing techniques and semiconductor material etching.

4. That I understand five United States patents have been identified as prior art reference patents possibly precluding the issuance of our captioned STIFFENED BACKSIDE FABRICATION FOR MICROWAVE RADIO FREQUENCY WAFERS application as a Letters Patent of the United States in view of the obviousness provisions of 35 U.S.C. 103(a). These references include a United States Patent 6,358,762 of Kohno et al. that was filed in the United States on March 23, 2000, (with claim of a Japanese Priority Date of September 27, 1999) and issued on March 19, 2002.

4. That I am familiar with the subject matter of the attached Exhibit 1 date-redacted pages from a US Air Force Laboratory Notebook that I maintained while employed by the U.S. Air Force at Wright Patterson Air Force Base, Ohio. The Exhibit 1 papers include about six drawing sketches or diagrams that I personally made while working at on the invention leading to the captioned application for Letters Patent of the United States.

5. That the redacted dates appearing in the left margin areas of these pages are in fact dates on which I, with my co-inventor colleagues, had performed certain experiments and trials that ultimately arrived at significant concepts recited in our captioned application for Letters Patent of the United States.

6. That, as is evidenced by these laboratory notebook pages and the indicated but redacted dates thereon, I, and my co-inventor colleagues, did in-fact invent the subject matter of the instant application in the United States prior to the issue date of the Kohno patent.

7. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the captioned application or any patent issuing thereon.

Gregory C. DeSalvo — 29 Dec 03

Gregory C. DeSalvo
Baltimore, Maryland

Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Gregory C. DeSalvo et al. Group Art Unit: 2823
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DECLARATION UNDER 37 CFR 1.131

Honorable Commissioner of Patents and Trademarks

Washington, D. C. 20231

Sir:

I, Gerald B. Hollins, declare:

1. That I am employed by the United States Air Force in the U.S. Air Force Material Command Law Office, Intellectual Property Directorate located at Wright-Patterson Air Force Base Ohio 45433-6573. This employment is in the capacity of a Patent Attorney registered before the U.S. Patent and Trademark Office as is indicated below herein.

2. That in the course of this employment I perform the duties of drafting, and prosecuting before the U.S. Patent and Trademark Office, applications for Letters Patent of the United States of America on behalf of the U.S. Air Force and U.S. Air Force-related inventors.

4. That I understand five United States patents have been identified as prior art reference patents possibly precluding the issuance of the captioned STIFFENED BACKSIDE FABRICATION FOR MICROWAVE RADIO FREQUENCY WAFERS patent application that I prepared as a Letters Patent of the Untied States in view of the obviousness provisions of 35 U.S.C. 103(a). These references include a United States Patent 6,358,762 of Kohno et al. that was filed in the United States on March 23, 2000, (with claim of a Japanese Priority Date of September 27, 1999) and issued on March 19, 2002.

4. That in the course of preparing a response to an October 20, 2003 Office Action from the U.S. Patent and Trademark Office Examiner of the captioned application for Letters Patent of the Untied States I inquired of several of the named inventors of this application regarding the current availability of early drawing sketches identified in the patent disclosure form relating to the captioned application. In response to this inquiry one inventor, Dr. Gregory DeSalvo, the first listed of the inventors of the instant application, responded with an affirmative reply that was based on pages contained in a Laboratory Notebook he maintained while working at Wright Patterson Air Force Base. Copies of these pages in date-redacted form are attached as Exhibit 1 to the herewith accompanying declaration under 37 C.F.R. 1.131 document executed by Dr. DeSalvo.

5. That for legal reasons, including the ever present possibility of a Patent Interference Proceeding or future Litigation, I have caused the date redaction steps notable especially in the left column of these pages to be accomplished. Notwithstanding these redaction steps, I wish to certify for the present record that the redacted dates appearing on these pages, including the final page "last day" paragraph date are indeed dates prior to the

issuance of the above-identified United States Patent 6,358,762 of Kohno et al. that occurred on March 19, 2002.

6. Moreover I believe that the drawing sketches prepared by Dr. DeSalvo and appearing on these Exhibit 1 pages together with the accompanying textual notes evidence a substantial completion of the invention described in the captioned application for Letters Patent of the Untied States that I prepared. Notably these sketches include the backside wafer thinning, metallized via holes, backside guard ring or circumferential rib, orthogonal grid, and ICP or RIE etching concepts that are described in the captioned application. Additionally I believe these sketches represent work accomplished here at Wright-Patterson Air Force Base, Ohio, in the United States, on dates prior to the issuance of the United States Patent 6,358,762 of Kohno et al. on March 19, 2002.

7. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the captioned application or any patent issuing thereon.

Gerald B Hollins — 07 January 2004

Gerald B. Hollins, USPTO Registration 25,452 — Date

To remove ΔAvg, press [CUR] + [ABT] on Tencor

Cleanroom Notebook

Project

Name Greg DeSalvo Date

Volume 6 Notebook

From: [redacted]
To: [redacted]

End Temp = 21.4°C

Dektek etch step height: 8304 Å 8406.6 Å
8504.7 Å 8320.3 Å
8334.8 Å

Avg height = 8374 Å which gives $\frac{8374 \text{ Å}}{123 \text{ min}}$ = 68 Å/min

This value is slightly higher than expected, although it is within reason. The etch step was very square — a beautiful etch step profile, with no edge trenching.

[redacted] Working with Andy Walker to finish up plotting the DLTS mask pattern for backside grid RIE etching / thinning.

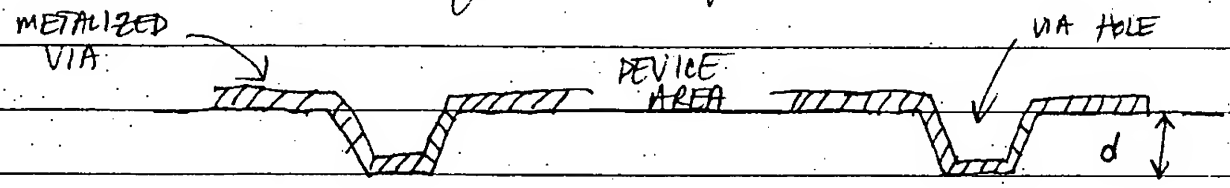
[redacted] Haven't had much time to work in the lab since I am leaving AFRL this Friday 10 Mar 00. Andy Walker has learned how to do digital etching on GaAs over the past few days & I hope he will be able to complete the work I did not do on my own. Also Andy will continue on with the backside etching of GaAs experiments using Cl_2 ICP RIE etching a/o any wafer mounting. This should be worth a patent for sure.

To close up this notebook, I will describe the basic backside processing that I (Greg DeSalvo), Tony Quach, Jack Ebel, & now Andy Walker have developed in theory.

X
Signature

Date

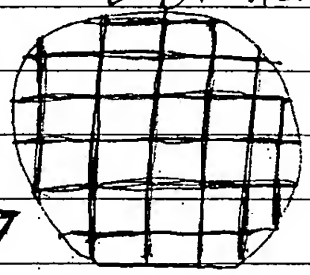
1. Perform normal frontside processing of either FET or HBT based MMIC circuit processing.
2. As part of the frontside processing, perform RIE (ICP) via hole etching FROM the FRONTSIDE, and metalize the via hole from the frontside



→ d = final desired thickness of wafer after backside thinning process

3. For backside processing align through wafer (IR mask aligner) and pattern for metal lift-off (or metal etch if necessary) a grid pattern where the saw street reticle frames will be on the frontside.
4. Metal deposit from evaporation or plating (sputtering) the metal needed to ask as an etch mask on the wafer backside.

< TOP VIEW of backside of wafer, showing "grid line pattern" representing where metal will be and aligned to topside reticle saw streets. Thickness of metal determined by etch mask needed. Width of metal = width of topside saw streets (≈ 75 μm)



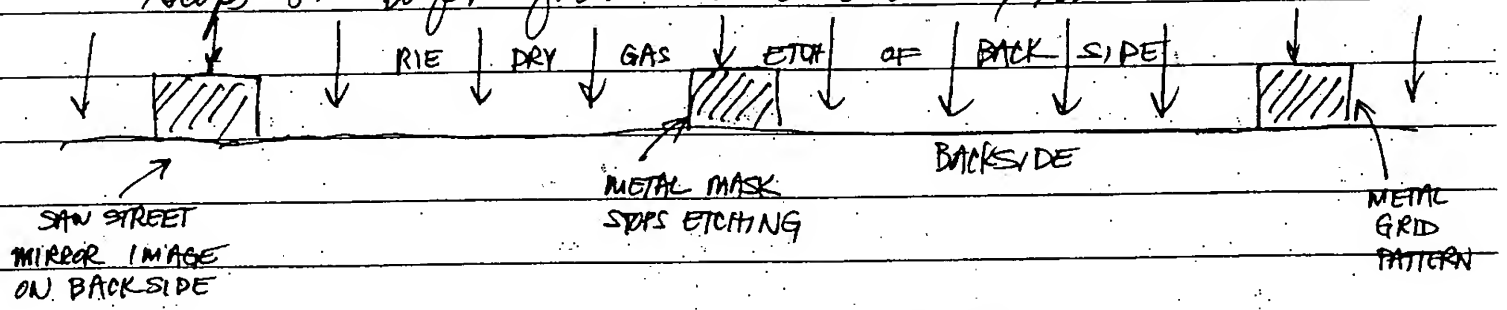
Let grid lines extend across wafer, even where no reticles have been exposed.

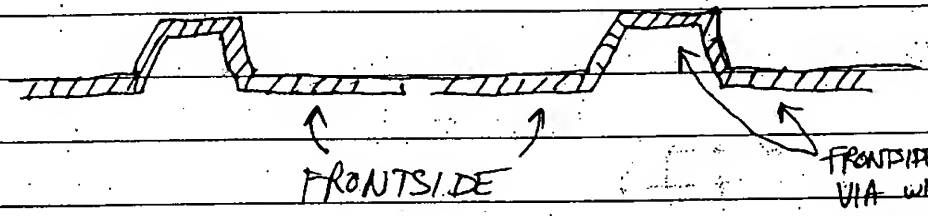
x
Signature

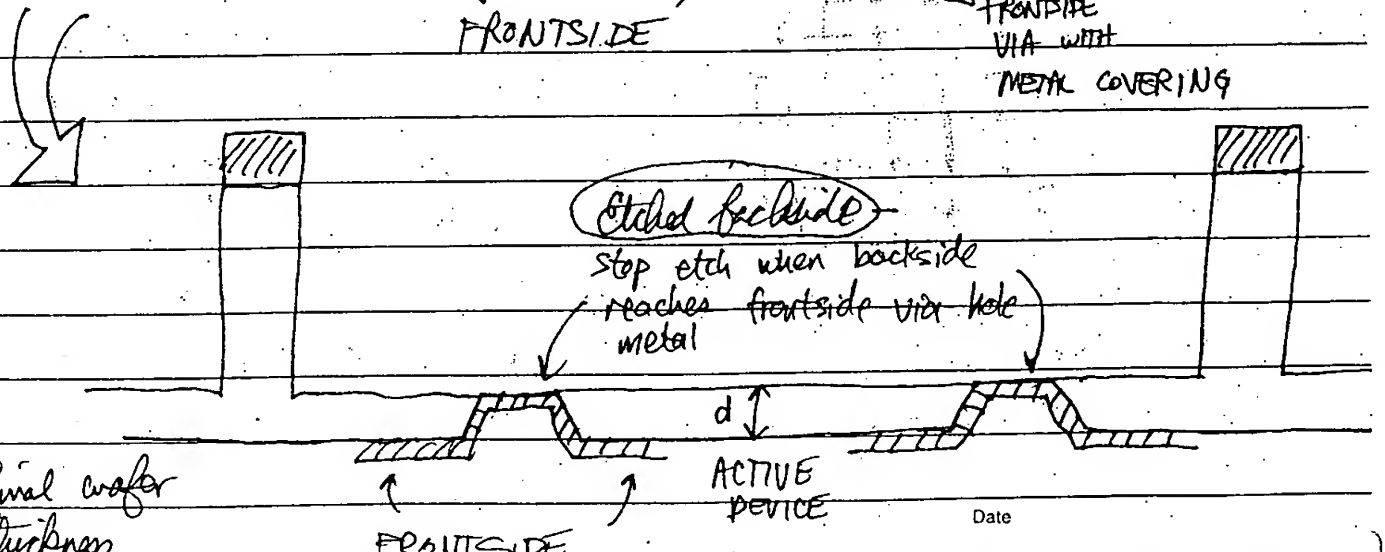
5. Perform backside wafer thinning by etching GaAs wafer (or potentially any other semiconductor wafer) using high density plasma reactive ion etching with a dry gas (e.g. ICP RIE etching with Cl_2 gas)

- No need to mount wafer onto sapphire or quartz carrier frontside down
- Load wafer frontside down into load lock ICP chamber and perform deep (~500 μm deep) etching of GaAs, using metal grid pattern on backside as an etch mask.

6. Etch backside of wafer until (anisotropically) etch selectively stops on wafer frontside via GaAs, such as







x d = final wafer thickness

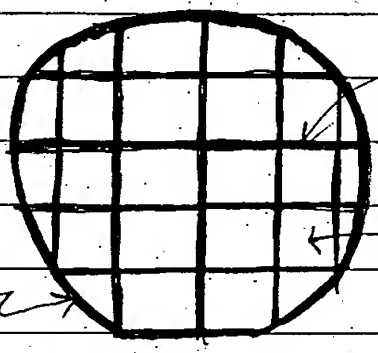
Signature

Date

7. Remove wafer from RIE chamber.
8. Blanket metalize backside of wafer
9. Wafer is complete from processing and ready for dicing, sawing, and packageng of chips in die.

- No need for wax mounting & demounting of wafer
- Fragile wafer is sturdied, strengthened by use of backside grid pattern of full wafer thickness ($\approx 600\mu m$) including guard ring around wafer perimeter due to ICP clamp masking etching of wafer perimeter

Backside view



metal grids (etch mask) unetched wafer underneath

(under active area device)

exposed wafer area etched down to thinned dimension (d) desired

unetched guard ring around wafer perimeter NOT metalized, but masked by ICP clamp surrounding wafer

Because of this grid pattern on the backside, the thinned wafer (e.g. $100\mu m$) is still rigid and strong since this grid pattern is not thinned ($\approx 600\mu m$) and the web maintains the original strength reasonably well. Therefore, no need for wafer mounting onto carrier for wafer thinning and structural support after thinning. The unetched guard ring surrounds and interconnects the metal grid pattern & strengthen the wafer on the outside edges

x
Signature

Date

Finally, the frontside via formation with frontside metal acts as a etch stop and a marker as to when the backside ~~wide~~ wafer thinning should stop, preventing or helping to prevent thinning the wafer too much.

[redacted]

Well, today is my last day at AFRL. It was a good run, & I got to work with a lot of good people. I hope my new job at Northrop Grumman will be as pleasant and fun as this one, but with increased opportunities to lead research projects and develop programs for the future.

X
Signature

Date